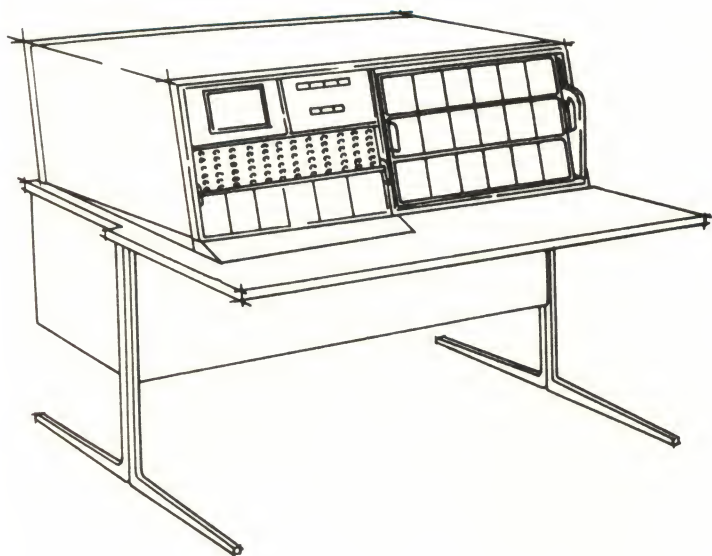


SIMULATORS INC.

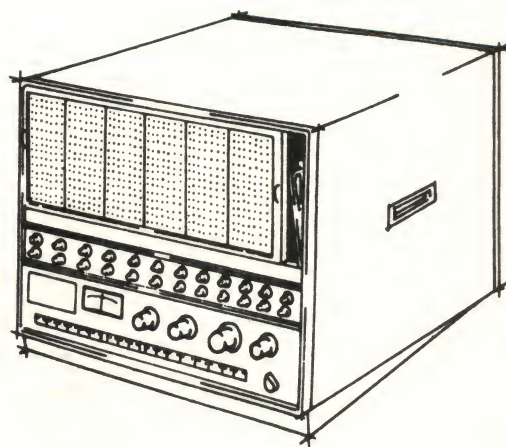
120

ADVANCED ELECTRONIC SIMULATION SYSTEMS

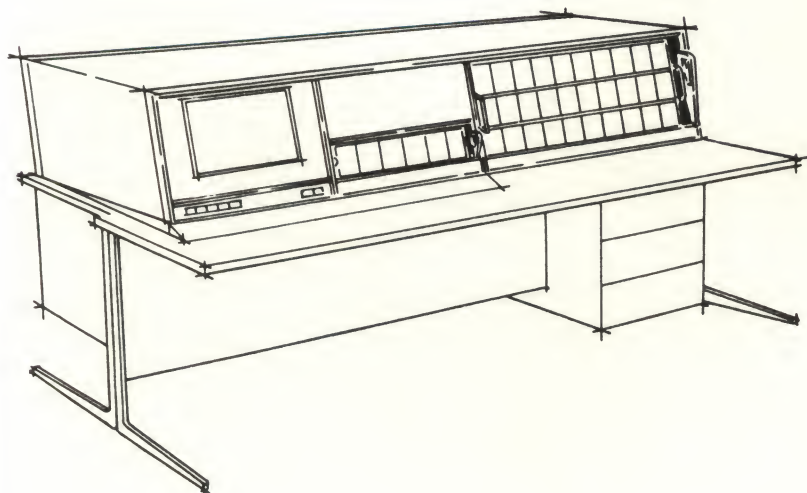
720 SIMULATOR



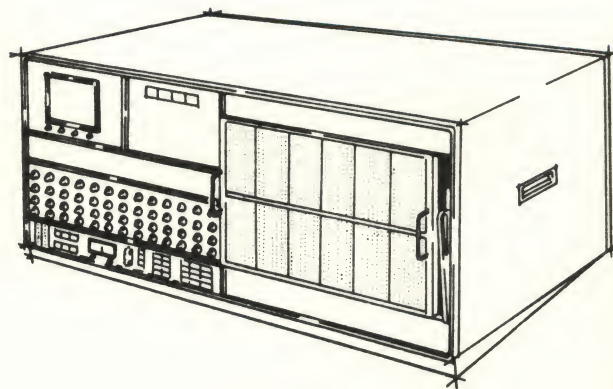
240 SIMULATOR



1440 SIMULATOR



480 SIMULATOR



LITERATURE ON THE 120 SERIES

Systems	Model 240 Simulator Model 480 Simulator Model 720 Simulator Model 1440 Simulator
Sub-Systems	12 PAK Sub-System, Control and Display Panel Electronic Digital Voltmeter Parallel Logic Electronic address and Servo Set Potentiometers Repetitive Operation Display Analog-Digital Computer Interface Power Supply, Type 801.0
Computing Components	Operational Amplifier, Type 1-510 Operational Amplifier, Type 1-620 EMC Integrator Networks, 2.000 group Multiplier, Type 3.110 Co-efficient Potentiometers, 7.000 group Logarithm DFG, Type 4.120 Sine-Cosine DFG, Type 4.510 Arbitrary DFG, Type 5.740 Logic Interface, 9.000 group
Programming Aid	SASI I Programming Method
Price Sheets	System and Component Price Sheets

THE 240 SIMULATOR

a precision general purpose analog computer

THE 240 SIMULATOR is a precision general purpose analog computer. Of an all silicon solid state design, the unit applies a modular construction to obtain a combination of high performance and flexibility. A sound fundamental technical design coupled with some unique packaging techniques offers the 240 Simulator user a choice of computing networks, accuracies and features to suit a wide range of applications.

A DESK TOP COMPUTER, the 240 Simulator has an expanded capacity of 28 operational amplifiers and a complete line of associated linear and non-linear computing components. The unit has features, accuracies and capabilities normally associated only with large simulation systems. The small size with large system features makes the 240 Simulator an excellent educational computer for the teaching of modern simulation principles.

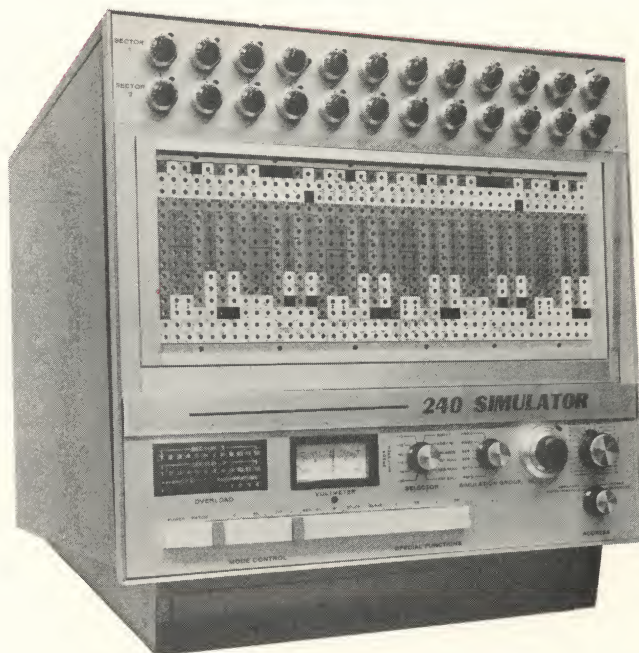
RELAY RACK MOUNTING capabilities allow the 240 Simulator to be easily integrated into an instrumentation laboratory. The wide range of available networks, the flexibility in equipment selection, and the numerous trunk lines establishes the unit as a capable general or multi-purpose instrument.

EXPANDABILITY is one of the major design criteria. The 240 Simulator benefits in being a member of the Simulators, Inc. Series 120 Advanced Electronic Simulation Systems, where within the series all components and most assemblies are physically interchangeable. The 120 family includes the 240, 480, 720 Simulator and 1200 Simulator. The 240 Simulator, by virtue of the 120 Series approach, may be expanded beyond the full equipment complement. A Simulators, Inc. trade-in policy allows low cost expansion to any 120 system. The purchaser, through the trade-in value, is able to obtain the most computing capability for a limited budget with full regard for expansion.

PROGRAMMING considerations play a large part in the 240 Simulator's overall ease of operation. The patch panel layout is based on a 12 amplifier group identified as the 12 PAK subsystem. Patching for all standard 12 amplifier groups is identical, thus the 240 Simulator is programmed essentially the same as all other Series 120 systems. Operational elements are color coded and arranged to follow normal analog computer program diagrams. In addition the SASI I (Software for Analog Simulation) programming aid is offered to complement the patching layout. SASI I assists the user in allocating equipment, patching, program scaling and general housekeeping. Programming concepts incorporated in the 240 Simulator are an asset to both the novice and experienced programmer.

MAXIMUM EFFICIENCY of problem run time is encouraged with the 120 Series approach to program setup and checkout. Every known feature has been implemented to eliminate the inconvenience and errors produced from post patching. Static check references are available at the patch panel. Integrator derivatives may be monitored through system address. Empirical functions are set independent of the patched program by use of a setup unit. Also co-efficient attenuators may be set externally by a digital voltmeter through use of the address buss. Efficiency or problem solution is a definite 240 Simulator design criterion.

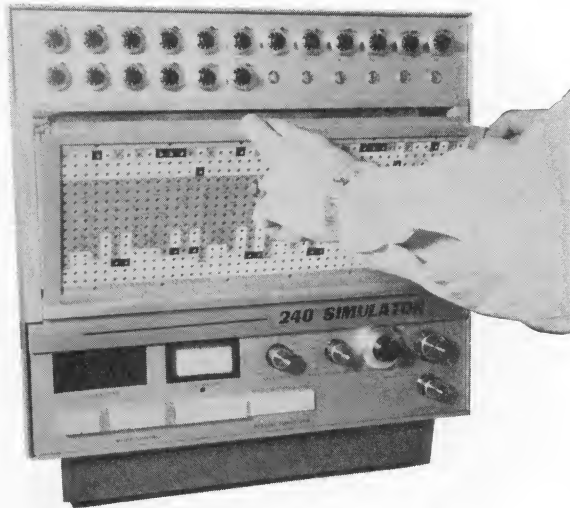
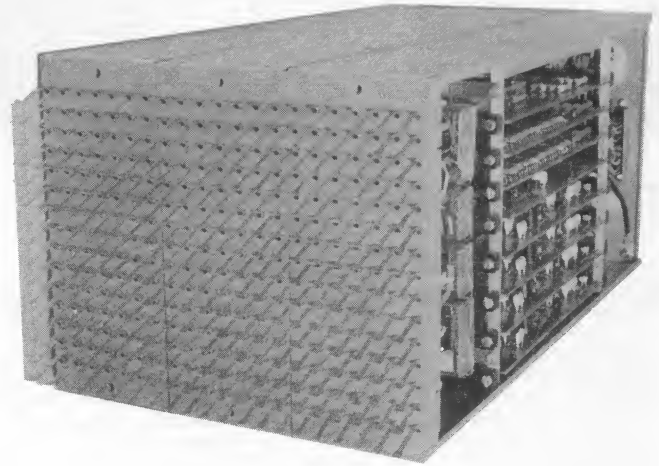
HYBRID COMPUTING considerations are everywhere apparent in the 240 Simulator. Electronic mode control with the optional feature of electronic hold, electronic switching of summers, track-store units, and high speed comparators all aid in hybrid and iterative problem solution. The Simulators, Inc. electronic digitally set attenuators are available as a standard system feature. The 240 Simulator is well prepared to implement hybrid computing techniques.



STANDARD EXPANDED SYSTEM CONFIGURATION

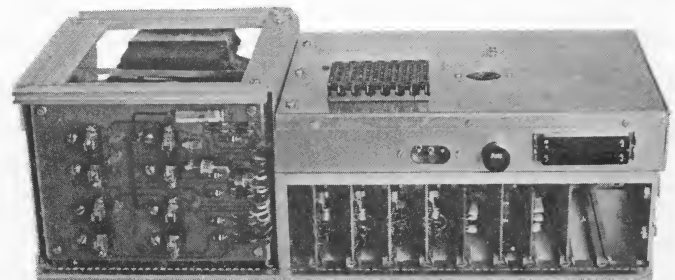
24	ea.	Operational Amplifiers w/summer inverter networks
12	ea.	Borrowable summer networks
24/30	ea.	Co-efficient Potentiometer
2	ea.	Electronic Digitally Set Attenuators
12	ea.	EMC Integrator Electronic Switching or Track Store Networks
4	ea.	Multiplier Networks
4	ea.	Fixed DFG Networks
4	ea.	Arbitrary DFG's (amplifier included)
2	ea.	Comparator Amplifiers
4	ea.	Active Limiters
2	ea.	3 pole Double Throw Function Relays
4	ea.	Push Button Function Switch
13/26	ea.	Trunk Lines

Current general purpose analog computers find increasingly diverse applications in widely varying scientific disciplines. Modern equipment needs impose a demand for flexibility in problem solving capability, system size and distribution of components. Simulators, Inc. has approached this difficult flexibility requirement through packaging the 240 Simulator in a modular construction. Computing components are housed in a four amplifier module (shown to the right) which, for performance considerations is positioned directly behind the patch panel. An assortment of available modules allows the user to select computing networks for a best fit of specific requirements. The removable modules are integrated into the system through the use of high quality connectors. High impact resistant orlon-filled diallyl phthalate block forms the patch bay. Removable computing components are installed into the module.

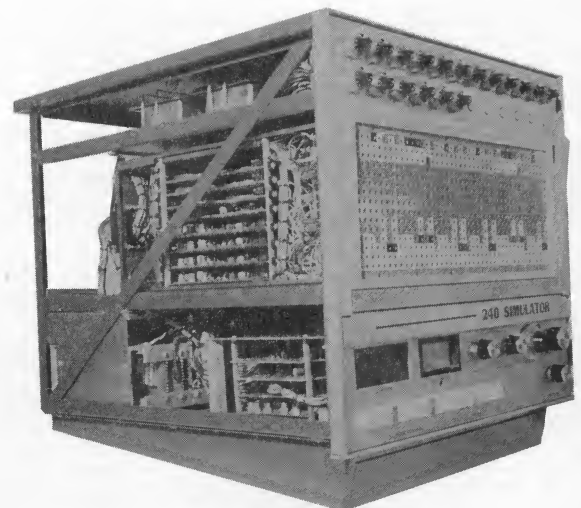


A removable pre-patch panel provides the means for analog computer program storage. A standard feature in all 240 Simulators, the patch panel is composed of a high dielectric diallyl phthalate selected for its low leakage characteristics. Gold plated patch cord tips mate with gold plated patch bay contacts. A wiping action imposed by the patch panel receiver design insures a positive low resistant contact. Patch bay contacts have a low angle of incidence and a wide blade to operate well with both prepatched programs and post patching. Patch panels are attractively color coded and are available to the user at the lowest possible cost.

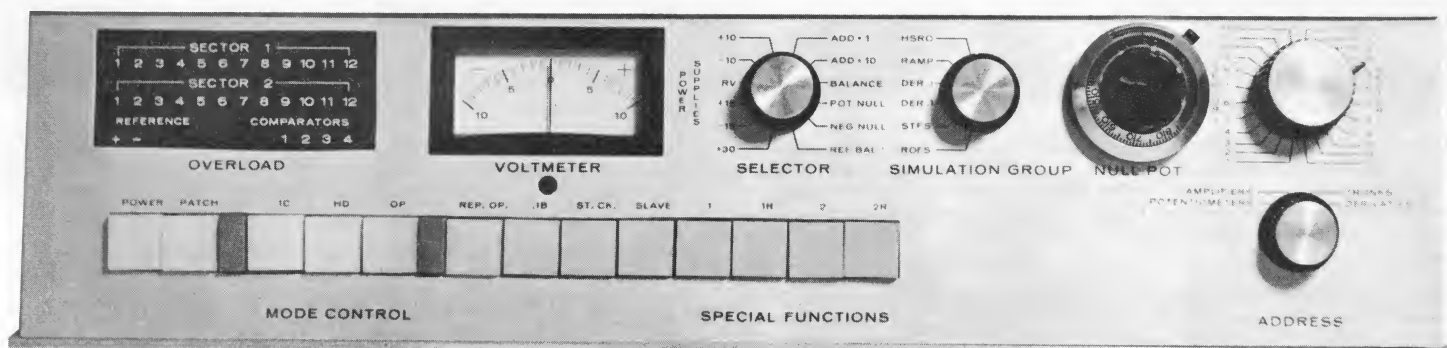
The 240 Simulator power supply design, the type 801.0, is a masterpiece of engineering for high performance and minimum maintenance. Of an all silicon design, the unit will withstand ambient temperature to 130° F. The wiring harness is layed out so that all test points are readily available for trouble shooting. Interchangeable regulator boards mounted in a printed circuit card file provide the maximum in maintainability. And even low cost protection is considered. The fuses are of the readily available inexpensive types commonly found in radio parts supply shops.



The 240 Simulator's maintainability is further accented by the ease of access to every component. In addition to the removable back plate, both side and top panels are easily removed. The side skin removal enables an access to every cubic inch in the system. Located directly under the top panel, integrating capacitors may be adjusted while the Simulator is in a standard operating configuration. The 240 Simulator is a compact design yet high in maintainability.



CONTROL AND DISPLAY PANEL



The 240 Simulator control and display panel presents a sophisticated push button control of system operations. Considerations for monitor, address and control appear on the panel from left to right, top to bottom, as follows:

MONITOR

OVERLOAD INDICATORS. The upper left position is the display for individual amplifier overload and comparator state indicators. Color coded lamps clearly indicate the overload status of all 24 system amplifiers and the two amplifiers committed for precision positive and negative reference. Also a light indicator for each comparator shows the existence of a "I" condition.

VOLTMETER. A $\pm 50\mu\text{a}$ sensitivity voltmeter is used to monitor power supplies and all system operational elements as either a DC voltmeter or nullmeter.

VOLTMETER SELECTOR. A rotary switch selector provides both monitor selection and voltmeter ranging. The table below shows the 12 selector positions and the full scale voltmeter needle deflection.

Position	Mode	Function	Full Scale Range ($\pm$)
Address x 1	Voltmeter	Monitor of address buss	10v
Address x 10	Voltmeter	Monitor of address buss	1v
Balance	Voltmeter	Monitor of address buss	50 mv
Pot Null	+Nullmeter	Monitor of address buss	50 mv
Neg Null	-Nullmeter	Monitor of address buss	50 mv
Ref. Bal.	Voltmeter	Monitor of pos. & neg. ref.	50 mv
+30	Voltmeter	Monitor of +30v power sup.	30v
+15	Voltmeter	Monitor of +15v power sup.	30v
-15	Voltmeter	Monitor of -15v power sup.	30v
RV	Voltmeter	Monitor of Relay power sup.	30v
+10	Voltmeter	Monitor of +10v Reference	10v
-10	Voltmeter	Monitor of -10v Reference	10v

EXTERNAL

Each 240 Simulator has a 21 pin connector located at the units rear. Output terminators are provided for external monitor of power supplies and the address buss. Reference, signal and relay ground and slave connectors are also available. The connector forms a convenient means of system output to read out equipment.

SIMULATION GROUP

The Simulation Group is a unique application of a chopper stabilized amplifier to a number of useful functions. The rotary switch control avails the user the following:

- HSRO** High speed repetitive operation control. Compute or operate timing unit is controlled by the Null Pot. The SG amplifier sweeps a ramp of -10 to +10 that may be used as a display oscilloscope time base.
- RAMP** The SG amplifier is programmed as a time base integrator with a -10 to +13.5 volt linear ramp output. 1C and OP are controlled from the "slow time" mode control, the ramp slope a function of the null pot setting. Output may be used as an XY plotter or oscilloscope time base.

- DER .1** The SG amplifier is used to monitor integrator derivatives and the electronic digitally set attenuator. The .1 scaling is a convenient readout of derivatives equivalent to $\pm 10 - \pm 100$ volts value.
- DER 1** Same as above except 1 scaling is for derivatives of values less than $\pm 10\text{v}$.
- STFS** The SG amplifier is programmed as a static function generator setup unit independent of the patch panel. Through use of the null pot and SG amplifier a manual sweep of -10 to +10 volts serves as the ADFG input. Read out of the function is conveniently obtained through an XY plotter or DVM.
- ROFS** "RO" indicates a rep op ADFG setup for use with the oscilloscope display. A -10 to +10 ramp from the rep op timing unit is used as the ADFG input. The entire ADFG function may be displayed for setup purposes.

ADDRESS

The 240 Simulator address is a 24 position rotary switch that provides address for amplifier outputs, potentiometer wiper arms, trunk inputs, integrator derivatives, ADFG outputs, and the electronic digitally set attenuators. A selector switch identifies the function and the 24 position rotary switch selects the unit. Address is by function, sector and unit.

MODE CONTROL

The 13 lighted push buttons are used to control system operations and special functions. From left to right the operation of each push button is described as follows:

- POWER** 110v 60cps AC power switch for all power supplies.
- PATCH** Energizes balance and pot set buss. All patch panel inputs to amplifiers are separated from the amplifier and grounded. Amplifiers are in the high gain balance configuration. Patch panel reference terminations are deactivated. Potentiometer inputs are removed from the patch panel program and connected to the 10 volt reference for setting co-efficients.
- 1C** Slow time initial condition integrator mode control, momentary "feather touch" type push button.
- HD** Slow time integrator hold mode control. May be used for relay or electronic hold. Momentary type push button.
- OP** Slow time integrator operate mode control Momentary type push button.
- REP. OP.** Energizes repetitive operation time scale buss and enables rep op timer.
- .IB** Console time scale provisions. All integrator time scales increased by 10 factor in both slow time or repetitive operation.
- SLAVE** The 240 Simulator is made the slave of a master unit.
- ST. CK.** Static check mode for program check procedures. Static check reference placed to specific patch terminations only in this mode.

SPECIAL FUNCTIONS Push buttons may be used; as analog function switches (single pole double throw terminations at the patch panel); to activate a function relay; or for other functions such as an enable for automatic hold in overload.

CONTROL OPERATIONS

AMPLIFIER BALANCE. Balance potentiometers for all 24 amplifiers are located under the decorative flap at the control panel. To balance an amplifier the voltmeter selector is placed in the "BALANCE" position. The amplifier is addressed and nulled to a balanced condition.

ATTENUATOR SETUP. In the patch mode all potentiometer inputs are removed from patch panel terminations and switched to positive reference. The "POT NULL" position of the voltmeter selector arranges the voltmeter as a positive nullmeter. Potentiometers are addressed and nulled to the "NULL POT" setting.

REP OP COMPUTE TIME CONTROL. The "NULL POT" controls compute time for the "REP OP" mode. Compute time varies inversely with the "NULL POT" setting, a unity setting equals 10 ms.

OUTLINE OF FEATURES

MODE CONTROL

Push button illuminated momentary and alternate action switches.

MONITOR

50u amp voltmeter furnished with the system. Address designed for DVM monitor. Ample trunks for other readout equipment. Individual amplifier overload and comparator state indicators are provided.

ADDRESS

Rotary switch address of amplifiers, potentiometers, trunks, ADFG's, Digitally set attenuators and integrator derivatives.

OPERATIONS

Patch mode for amplifier balancing, program patching, attenuator setup, and patch panel removal.

Repetitive Operation Mode for oscilloscope display of problem solutions. (75 solutions per second maximum rate) Ramp output from Simulation Group amplifier used as oscilloscope time base.

Console Time Scale for increasing time scale of all integrators by 10 factor.

Static Check Mode for ease of static check procedures.

Slave Mode for control of the slaved 240 Simulator by a master computer or device.

Derivative monitor of all integrators. Derivative readout through the Simulation Group Amplifier in HD and IC or HD and OP mode.

Function Generator Setup Unit allows ADFG to be set up independent of the patch panel input. A function may be set up statically through use of a plotter or DVM, or in repetitive operation through use of an oscilloscope.

PERFORMANCE

POWER SUPPLY-175 watt unit may operate 64 amplifiers. All fuses inexpensive, easy to replace.

REFERENCE-Positive and negative 10 volts, 300 ma output each. .01% regulation with .005% tracking. Monitor of positive and negative reference balance.

PATCH PANEL-Gold plated cords mate gold plated patch bay contacts with good wiping action.

AMPLIFIERS-All silicon solid state, low offset, low noise, short time recovery from overload with good dynamic characteristic.

ADFG SETUP. ADFG's may be set statically where a DVM or plotter is used to monitor input and output - or dynamically through use of the repetitive operation oscilloscope. All ADFG's have a toggle switch that removes the patch panel input and places the input on the SIMULATION GROUP amplifier output buss. In the static setup the ADFG input is determined by the NULL POT setting. The SG amplifier varies linearly with the NULL POT from -10 to +10 volts. The ADFG outputs may be monitored through the system address. The rep. op. setup utilizes a repetitive operation sweep as the ADFG input where the ADFG output may be monitored for a overall visula display of the empirical function.

LIMITER SETUP. Active limiter potentiometers are located under the decorative flap alongside the balance potentiometers. A positive and negative pot is supplied. The amplifier to be limited is monitored for desired limit conditions.

DERIVATIVE MONITOR. When the 240 Simulator is in the HD mode, the address function selector positioned to "Derivative" and the SIMULATION GROUP positioned to either DER I or .I, (depending on derivative value), the inverted integrator derivative will appear on the address buss. Readout may be through the nullmeter or external device.

INTEGRATORS-Electronic mode control, Electronic hold option. Up to 5 times scales per integrator available. All adjustable polystyrene capacitors.

ATTENUATORS-Composition or wire wound option. Wire wound 5K ohm resistance, .01% resolution.

MULTIPLIERS-To .013% FS accuracy. Exceptional small signal accuracy. Good dynamic characteristics.

ARBITRARY DFG's-10 segment variable slope, variable break point, switch for parallax, Gain and initial slope adjustment. Adjustments have knobs w/indicator and scale setting.

COMPARATORS-High sensitive amplifier with digital output and complement.

LIMITERS-Active hard limit. Positive and negative potentiometers furnished with each unit.

PROGRAMMING

SASI I (Software for Analog Simulation I) programming aid and training kit furnished to 240 Simulator users.

MAINTENANCE CONSIDERATIONS

Modular construction

Removable Top & Side Panels

All silicon solid state components, no germanium used

All electronic components distributor catalog items. No hous numbers.

FIELD SERVICE REPLACEMENT PROGRAM

Practically all 240 Simulator maintenance may be handled through the Replacement Parts Program. Should a component be inoperative, the user notifies the Simulators, Inc. factory to rush, within 24 hours, a replacement part. The user keeps the replacement part, which will have been refurbished to new equipment standards, the defective part retained by Simulators, Inc.

WARRANTY

All 240 Simulators are furnished with a full one year warranty. Simulators, Inc. will repair under the Replacement Parts Program, at no cost to the user, any cause of defective operation. The one year warranty covers all normal operation; however, excludes obvious operator abuse to the system.

SIMULATORS INC.

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Phone (312) 272-6310

12 PAK SUB SYSTEM

DESCRIPTION

THE 12 PAK SUB SYSTEM is a 12 amplifier group of analog computing components common to all Simulators, Inc. Series 120 Advance Electronic Simulation Systems. It is a complement of equipment selected for a flexible, well rounded distribution of operational amplifiers and their associated linear and non-linear networks.

AS A SECTOR of the 120 Series Simulators the 12 amplifier group provides a series identity and a common patching layout for both small and large systems. Operational element locations and patching are standard for all systems. The approach has the advantage of facilitating initial orientation to any of the 120 systems as well as providing a convenient breakdown of components for programming ease.

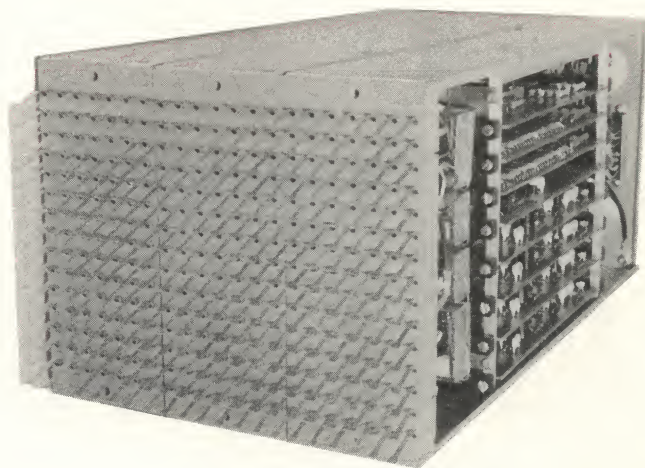
ALL SERIES 120 SIMULATORS are multiples of the 12 PAK sub-system. The 240 Simulator has two each 12 PAKs, the 480 Simulator-four each 12 PAKs and the 720 Simulator has six each 12 PAKs.

ADDRESS of a computing component or trunk lines is one of sector or 12 PAK identification and address of the unit within the sector. For example amplifier 3 of Sector 2 is addressed A2/3. Pot 12 of Sector 5 would be addressed P5/12.

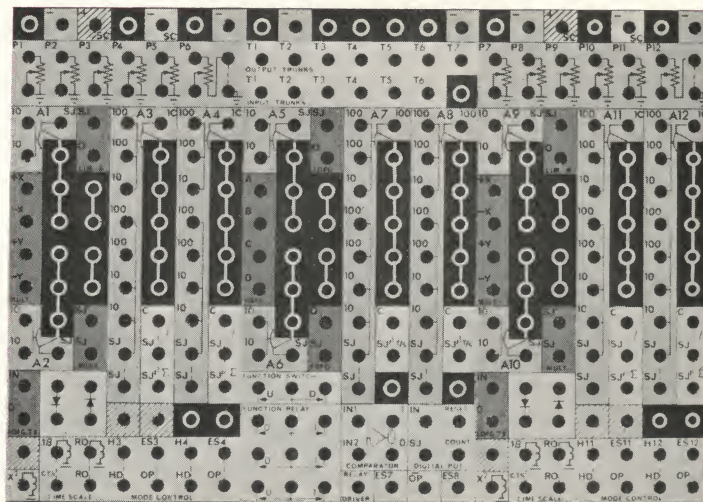
THREE NETWORK AND COMPONENT MODULES comprise the 12 PAK sub-system. The modules house four amplifiers, computing networks and summing resistors, as well as provide feed-throughs for trunks, attenuators, ADFG's, etc. There are two basic modules with variations for packaging flexibility. The standard 12 PAK complement incorporates two identical modules having integrator and multiplier provisions for amplifiers 1-4 and 9-12. The middle module, amplifiers 5-8, contains a logic interface and the fixed diode function generators. The computing components may be allocated as follows:

STANDARD 12 PAK CONFIGURATION

- 4 ea. Summer-Integrators
- 2 ea. Summers w/electronic switching
- 6 ea. Summer-Inverters
- 12 ea. Co-efficient Potentiometers
- 1 ea. Electronic digitally set attenuator
- 2 ea. Multipliers
- 2 ea. Arbitrary Diode Function Generators with included amplifiers
- 2 ea. Fixed Diode Function Generators
- 1 ea. Comparator
- 2 ea. Track and Store Units
- 1 ea. 3 pole double throw function relay & driver
- 1 ea. Function switch terminations
- 2 ea. Hard Limiters
- 4 ea. Free Diodes
- 13 ea. Trunk lines



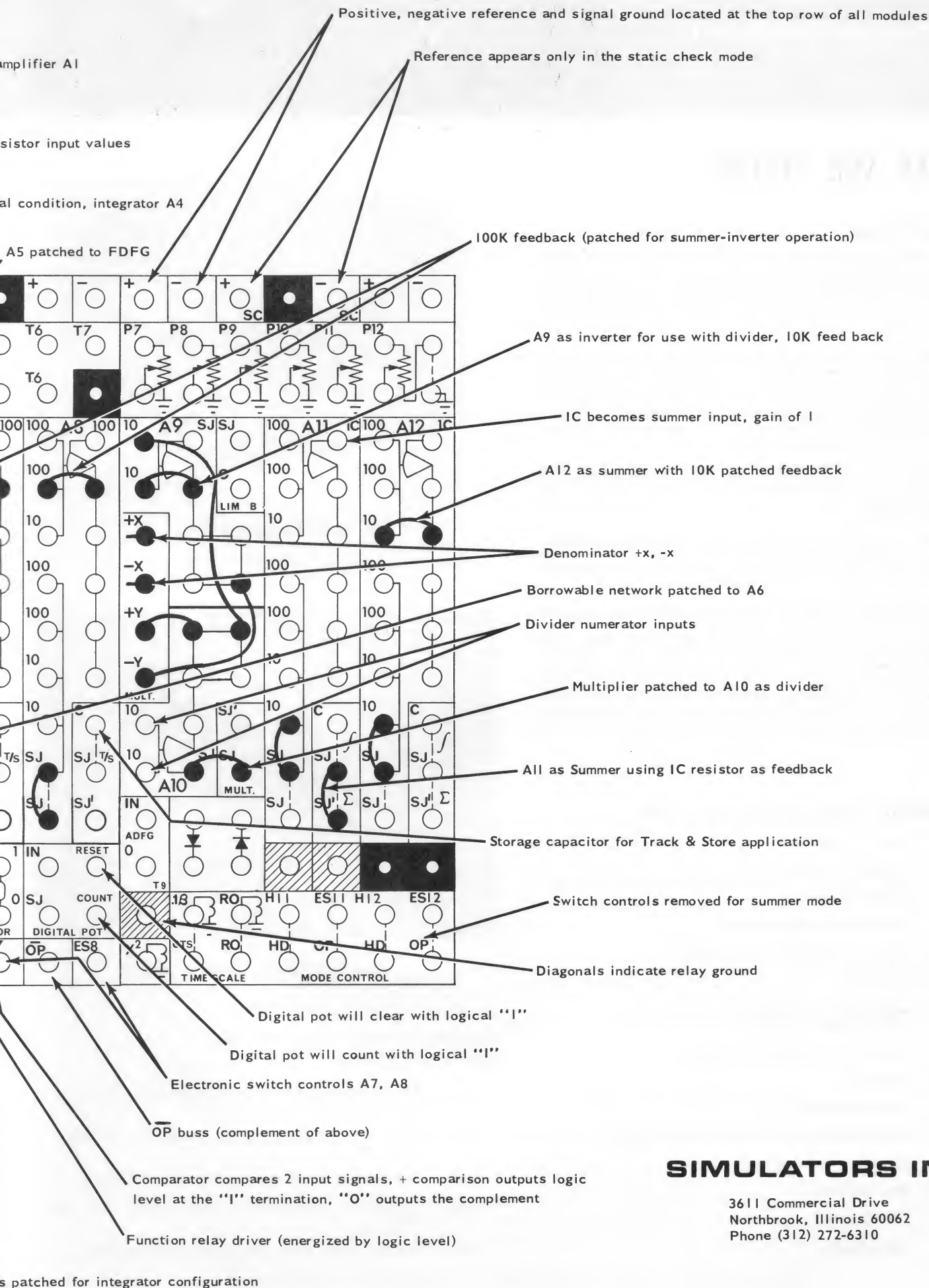
12 PAK SUB-SYSTEM



12 PAK SECTOR ON PATCH PANEL

ALTERNATIVES TO STANDARD CONFIGURATION

- 2 ea. Summer-Integrators may replace the summers w/electronic switching
- 1 ea. Multiplier may replace 2 ea. Fixed diode function generator
- 2 ea. Fixed diode function may replace 1 ea. Multiplier
- 6 ea. Co-efficient potentiometers may replace 13 trunk lines
- 2 ea. Summers may replace 2 ea. Summer-integrators

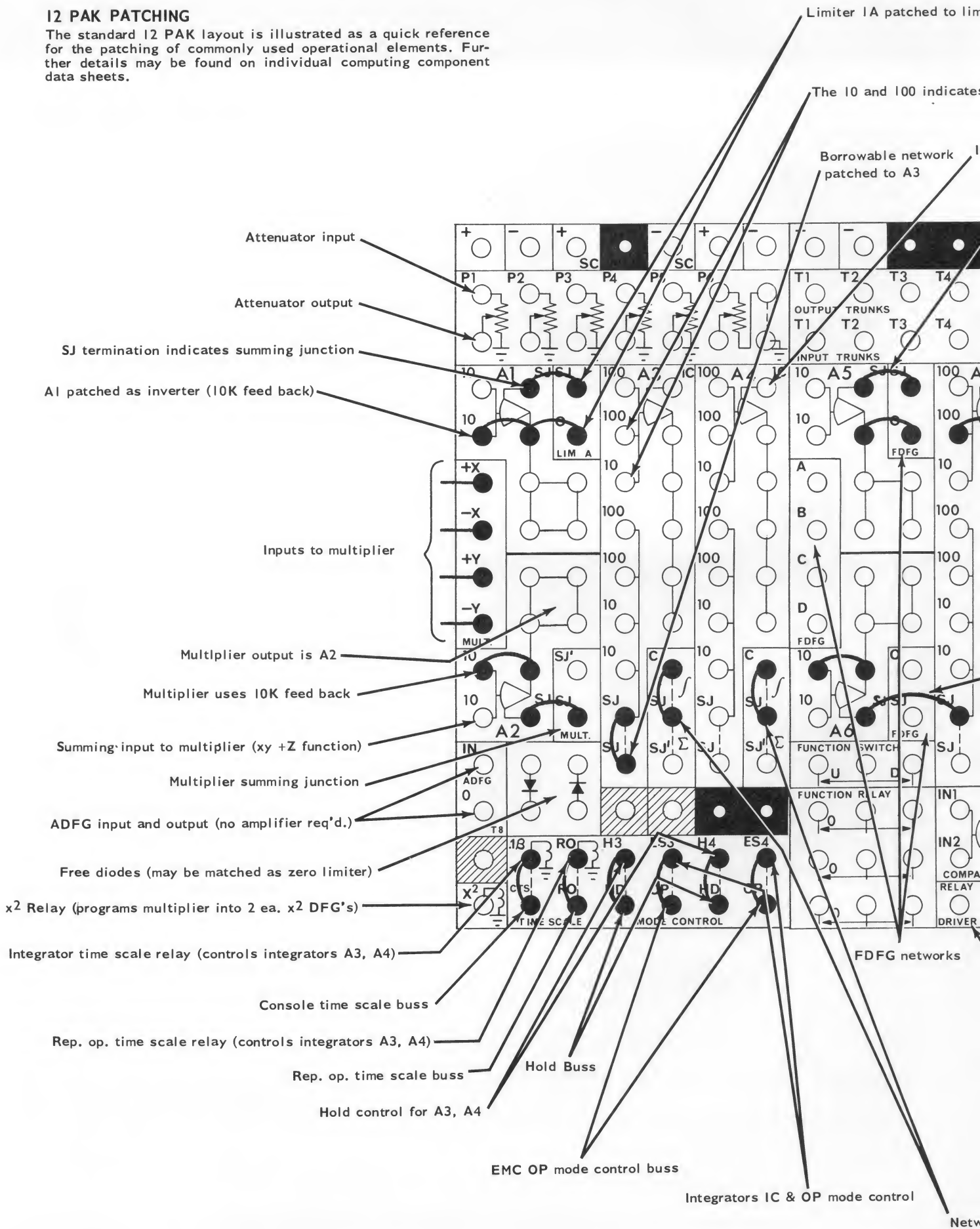


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12 PAK PATCHING

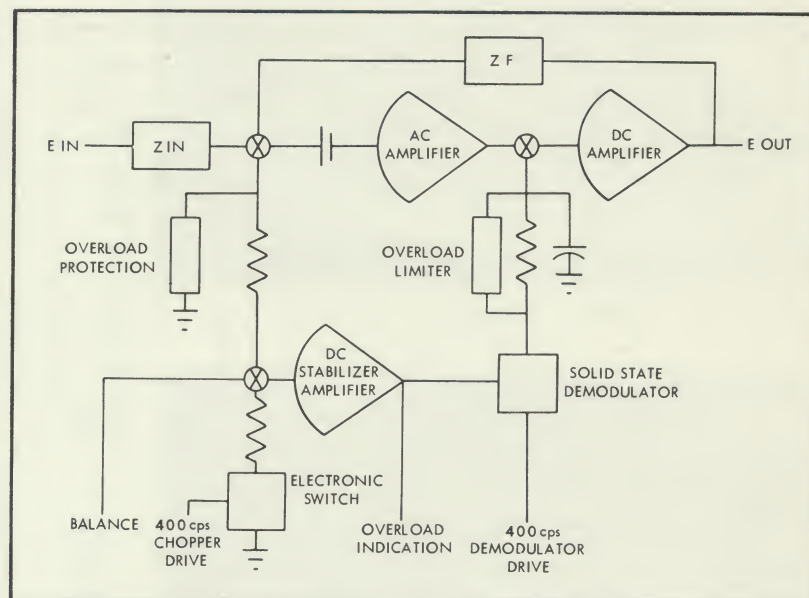
The standard 12 PAK layout is illustrated as a quick reference for the patching of commonly used operational elements. Further details may be found on individual computing component data sheets.



OPERATIONAL AMPLIFIER, TYPE 1.520

FEATURES

- Silicon Solid State Design
- Solid State 400 cps Chopper
- High Current Output
- Excellent Capacitive Loading Characteristics
- Low Summing Junction Offset
- Short Time Recovery from Saturated Overload
- Low phase shift at high frequency operation
- Excellent overall dynamic characteristics
- Low 60 cps pick-up
- High signal-noise ratio



SIMPLIFIED SCHEMATIC OF THE TYPE 1.520 DC
OPERATIONAL AMPLIFIER

DESCRIPTION

THE TYPE 1.520 OPERATIONAL AMPLIFIER is a high performance solid state design of a quality to excel in the widely varying requirements of modern analog and hybrid computing. A sound basic approach and some unique circuitry provides both accurate low drift slow time and excellent high frequency operation. The 1.520 amplifier blends gain and roll-off with outstanding chopper stabilization to yield exceptional system performance.

LOW FREQUENCY or slow time simulation is traditionally the analog computer's major function. Accurate differential equation solution is primarily dependent upon the computer's low frequency (.1 to 10 cps) performance. An analog system must have an operational amplifier that delivers high uniform gain, low phase shift, a large signal to noise ratio, low summing junction offset while maintaining good stability throughout the low frequency range. The 1.520 amplifier has been carefully designed to meet precision slow time computing criteria.

CHOPPER STABILIZATION effectively eliminates DC amplifier drift. Its use, however, can have undesirable side effects. If the stabilizer section has a large time constant, it inherently produces a large low frequency phase angle. The result is an unexpected slow time gain loss and phase shift increase. To reduce the demodulator time constant, an amplifier must employ a high frequency stabilizer. The 1.520 amplifier applies a 400 cps chopper to absolutely minimize slow time computing errors.

400 CPS CHOPPER FREQUENCY also serves to reduce 60 cps pick-up. The stabilizer operates at the desirable seventh harmonic of the ubiquitous AC power frequency. Beat with and pick-up of 60 cps spurious signals is almost eliminated in the Type 1.520 amplifier.

THE SOLID STATE CHOPPER enables the stabilizer to operate at high frequencies without the reliability problems of a mechanical chopper. The solid state chopper employed in 1.520 amplifiers is precisely controlled by a timing sequence that best suits stabilizer operation.

LONG TIME RECOVERY from overload conditions is both a

nuisance and handicap to the analog computer. The 400 cps chopper frequency, along with a unique stabilizer limiting circuit, provides the 1.520 amplifier a fast return from saturated overload.

HIGH INPUT IMPEDANCE to the DC and stabilizer sections is imperative for low amplifier input current. As input current is critical to the amplifier's application as an integrator, minimum input current has been a major criteria for the 1.520 design. The unit uses a differential input stage, a low leakage blocking capacitor and high stabilizer input impedance. The 1.520 amplifier provides unsurpassed performance as an analog computer integrator.

AMPLIFIER BALANCE or the adjustment of summing junction offset directly effects the amplifier's performance as an integrator. A poor balancing technique results in undesirable integrator drift. In all Simulators, Inc. systems the 1.520 amplifiers are balanced in a high gain configuration (large feedback resistance), the only method to absolutely minimize summing junction offset.

CAPACITIVE LOADING characteristics provide an indicator of an amplifier's stability in system operation. Marginal capacitive loading capability may result in amplifier oscillations. Distributed capacitance loading on both the summing junction and output and the amplifier used as an electronic mode control integrator may cause a decided loss of performance. The 1.520 amplifier exhibits a stability that insures uniform accuracies under relatively severe capacitive loading.

EXCELLENT DYNAMIC ACCURACIES are a feature of the Type 1.520 design. Open loop gain at the 1KC operating range is maintained at a high level. Phase shift is such that gain and phase shift errors are compatible. Compensation of input and feedback networks are not required allowing for consistent accuracies with widely varying patching configurations.

OVERALL the Type 1.520 operational amplifier incorporates every known technical advance to provide analog and hybrid computing the highest level of performance.

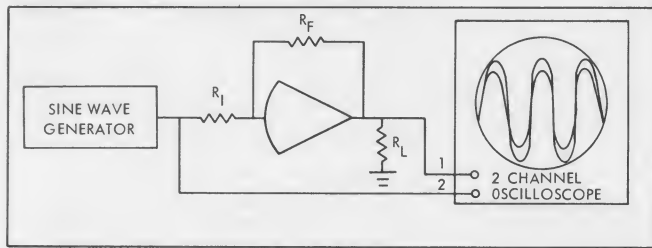
ELECTRICAL CHARACTERISTICS

TEST PROCEDURE

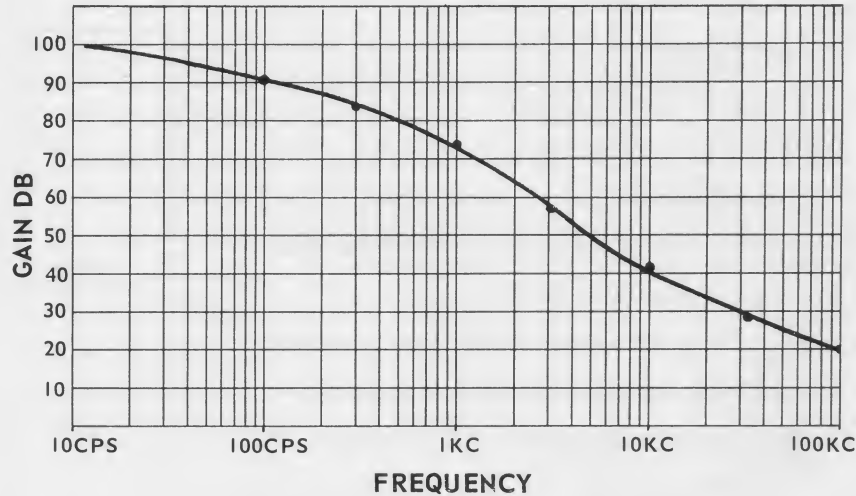
TEST RESULT

OPEN LOOP GAIN

Frequency response characteristics of an operational amplifier provide an insight to the amplifier's stability as well as performance in high frequency operation. The classic roll-off slope of 20 db/decade indicates that the circuit is essentially first order with little tendency toward oscillation or peaking. The 1.520 amplifier frequency response follows closely the 20 db/decade slope while maintaining the gain required for high speed computing. The 74 db gain at the 1KC operating range yields a gain error of less than .015%.

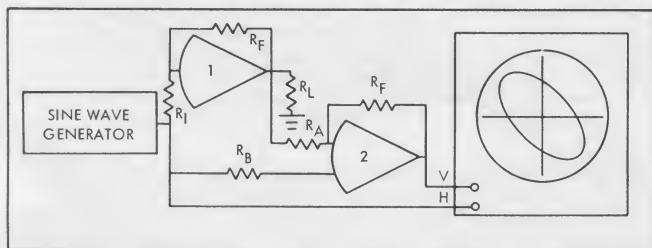


Open loop gain may be obtained through the above test setup. The ratio of input less output divided by input shows the closed loop error due to open loop gain loss. Open loop gain (in decibels) is approximated from its reciprocal to be $20 \log \frac{E_{in}}{E_{in}-E_o}$.



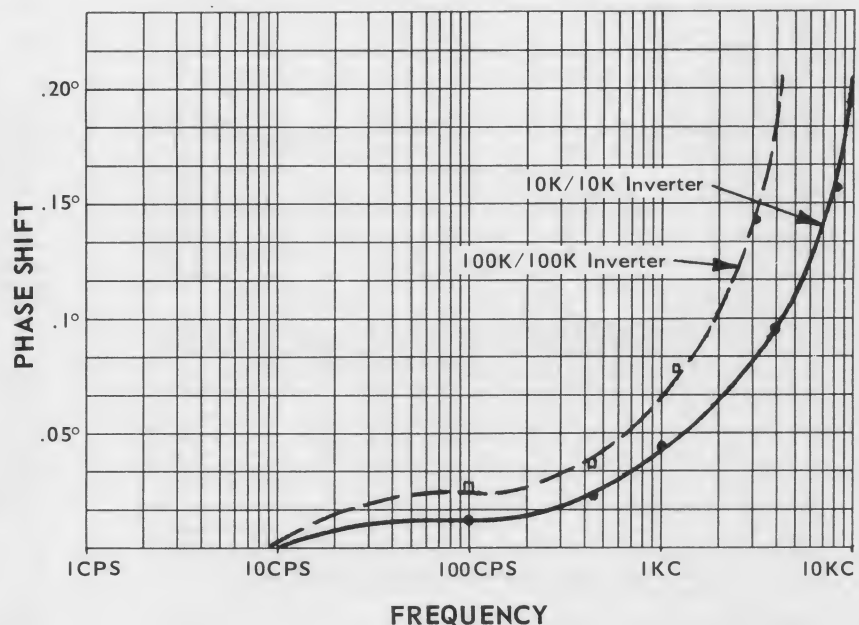
PHASE SHIFT

As a rule, phase shift is the most limiting factor to accurate high frequency operation. For example, a phase angle of $.1^\circ$ has a sine or error of .3%. Phase shift is a function of amplifier design, system packaging, and network impedances. The illustrated phase angle vs frequency curves are for the Type 1.520 amplifier as packaged in all Simulators, Inc. systems. Input and feedback resistors are the Simulators, Inc. standard, and as with all standard Simulators, the resistors are uncompensated. Curves are from data measured at the patch panel with the amplifier patched as an inverter.



The above circuit may be used to measure phase shift. A sine wave input to the amplifier under test is also summoned with the amplifier output. A lissajous figure of error vs. sine wave input will display phase angle error. The error may be measured at the Y axis where $x=0$ or 180° . Phase angle is the arc sine of error $\div$ input.

Care must be taken to match impedances of R_A and R_B else any discrepancy may be interpreted as amplifier phase error. R_A and R_B should be reversed and the two readings averaged.



Attention is called to the monotonic characteristic of the of the above phase shift curves. Phase shift is shown to increase with frequency at close to a constant rate, an indication of sound amplifier design and packaging techniques.

ELECTRICAL CHARACTERISTICS

TEST PROCEDURE

TOTAL DYNAMIC AMPLITUDE ERROR

The overall dynamic amplitude error is a combined phase shift and gain error. It is generally specified at the 1KC frequency operation with the amplifier patched as an inverter.

Total dynamic amplitude error may be found from the same lissajous figure used to determine phase shift. Where phase shift is measured only at the Y axis (the input sine wave being 0° and 180°), total dynamic error is the maximum error amplitude that may occur over the entire input range.

VELOCITY LIMIT

Velocity limit is the maximum rate at which an amplifier may pass a signal. It is generally expressed in volts/sec. and indicates to the user a high frequency operating limit for full scale use of the system.

A saw tooth wave input to an amplifier patched as an inverter will provide a quick velocity limit check. Holding a constant frequency the saw tooth amplitude is increased until a limit is detected.

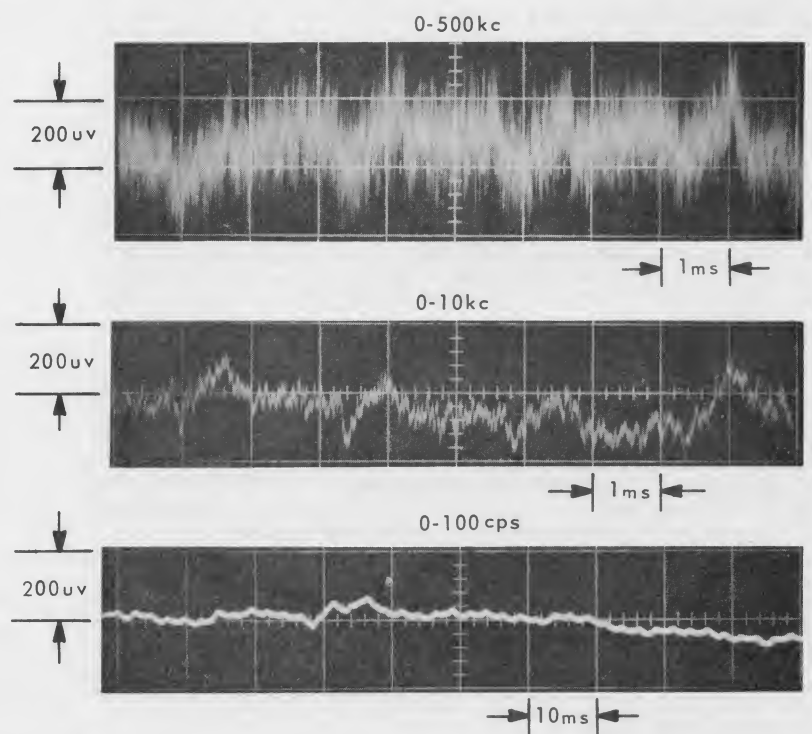
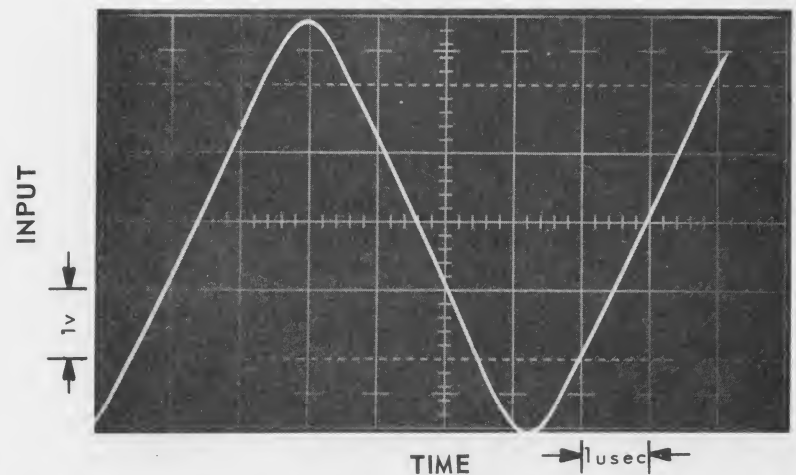
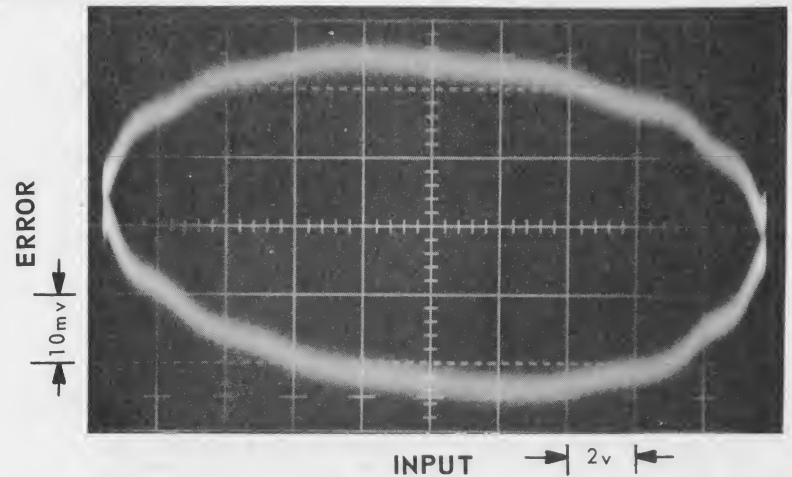
NOISE

Amplifier noise is an undesired complex output superimposed on normal operating signals. Its origin is mainly from circuit components, power supply and ground noise, and chopper drive.

Characteristics may be listed in both RMS (root mean square) and/or peak amplitude, referred to the running junction. The RMS specifications are preferred by many manufacturers as their values may be considerably lower than those given for the same amplifier in peak noise figures. Also RMS specifications may hide relatively large narrow spikes (such as those resulting from the chopper). Both RMS and peak noise specifications are listed for the I.520 amplifier to show that chopper spikes do not exert a noticeable influence on the amplifier performance.

To fully evaluate the effect of noise on system accuracies, it is necessary to analyze the frequency components that comprise the overall wave form. By use of simple filters, it is possible to place various band widths on an oscilloscope. These may be photographed as shown on the attached I.520 noise measurements.

TEST RESULT

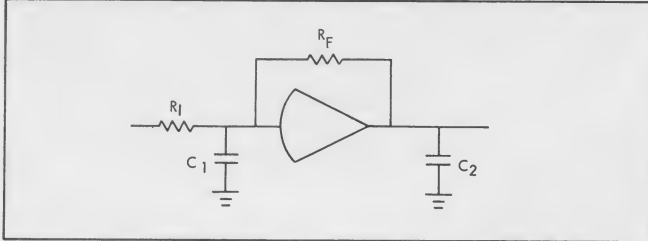


ELECTRICAL CHARACTERISTICS

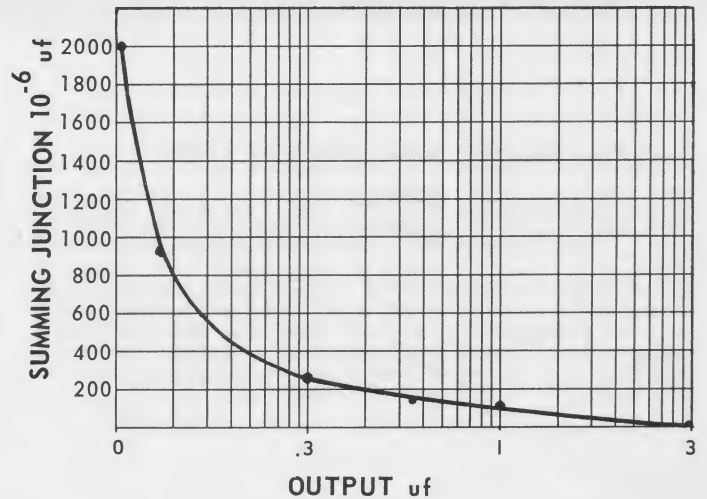
TEST PROCEDURE

CAPACITIVE LOADING

Capacitive loading characteristics of an operational amplifier are critical to the amplifier's system stability margin. Distributed capacitance that may occur in trunk lines, patch panel contacts, read out equipment, etc., can effect a marginally stable amplifier. Equally important, the large capacitive loading imposed by electronic mode control will severely handicap integrator performance if an amplifier does not function well under capacitive loads.

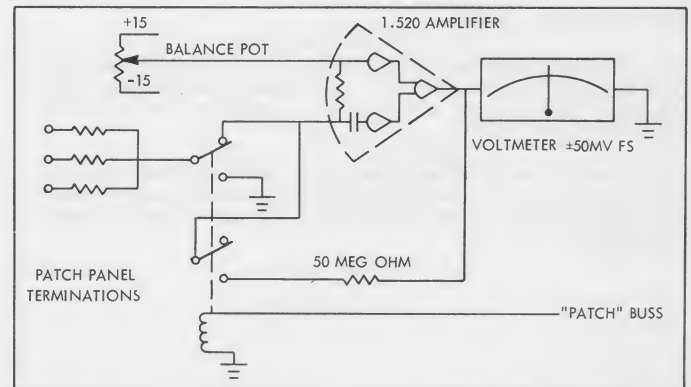


To evaluate the amplifier's capacitive loading capabilities, it is necessary to plot stability as a function of summing junction load (C_s) versus output load (C_o).



AMPLIFIER BALANCE

Amplifier balance for chopper stabilized amplifiers is generally accepted as the potential between the output and summing junction. When the amplifier is balanced, in effect the summing junction offset is biased such that the summing junction (and output) potential is brought as close as possible to system ground potential. Summing junction offset is usually the largest contributing factor to integrator drift; thus amplifier balance is highly important if accurate integration is to be expected.



SPECIFICATIONS

Linear operating range.....	$\pm 13.5 \text{ v}$
Output current @ $\pm 10\text{V}$ DC.....	$\pm 33 \text{ ma}$
Open Loop Gain (at DC).....	4×10^7
(at 100 cps).....	40,000
(at 1 KC).....	6,000
Bandwidth (-3db w/10k-10k).....	350 KC
(-3db w/100k-100k).....	175 KC
Phase shift (100 cps w/10k-10k).....	.008°
(1kc w/10k-10k).....	.05°
(100 cps w/100k-100k).....	.02°
(1kc w/100k-100k).....	.20°
Total Dynamic Error (1KC, 20vpp w/10k-10k).....	.1%
Velocity Limit.....	$2 \times 10^6 \text{ v/sec}$
Output Noise (Full bandwidth 10k-10k).....	200 μv peak
.....	125 μv RMS
(Full bandwidth w/100k-100k).....	800 μv peak
.....	500 μv RMS
Recovery from Saturated Overload.....	1.0 sec
Input Current.....	10^{-12} amp
Offset at the Summing Junction.....	0-3 μv
Capacitive Loading on Output to ground	
(w/100k-100k).....	.1 μf
Capacitive Loading at summing junction to ground	
(w/100k-100k).....	.001 μf
Stability - Feedback resistance.....	$0-\infty$
Stability - Input resistance.....	500 ohms- ∞
Output Impedance (100 cps).....	.01 ohm
Drift (Temperature).....	.5 $\mu\text{v}/^\circ\text{F}$

Size.....	2 1/2" x 5 1/2"
Power requirements	
.....	+15 -12 ma
.....	-15 -13 ma
.....	+30v - 5 ma
.....	8v AC-chopper

All specifications are for the 1.520 amplifier when packaged in any Simulators, Inc. 120 Series Simulator, recorded at the patch panel.

SIMULATORS INC.

3611 Commercial Drive
Northbrook, Illinois 60062
Phone (312) 272-6310

SERIES 120 COMPUTING COMPONENTS

NETWORK AND COMPONENT MODULE

.01% Resistors, Multiplier - Integrator provisions, Type 101.0.....	\$235.00
.01% Resistors, Same as Type 101.0 w/x ² programming relay Type 102.0.....	285.00
.01% Resistors, Logic interface - Integrator Provisions, Type 111.0.....	245.00
.01% Resistors, Logic interface provisions, Type 121.0.....	230.00

AMPLIFIERS

Operational Amplifier, Chopper Stabilized, Type 1.520.....	150.00
Operational Amplifier, Type 1.600.....	95.00

POTENTIOMETER

Attenuator Group, 6 ea composition potentiometers, Type 7.300.....	215.00
Attenuator Group, 6 ea wire wound potentiometers, Type 7.580.....	400.00

EMC INTEGRATORS

Dual Integrator network, 1 time scale, .1%, Type 2.000.....	355.00
Dual Integrator network, 2 time scales, .1%, Type 2.070.....	405.00
Dual Integrator network, 4 time scales, .05%, Type 2.220.....	635.00
Dual Integrator network, 4 time scales, .02%, Type 2.230.....	820.00
Dual Integrator network, 5 time scales, .02%, Type 2.540.....	875.00
Feature of electronic hold to any of the above dual networks.....	175.00

MULTIPLIERS

Multiplier Network, Type 3.110.....	595.00
Multiplier Network, "Guaranteed Typical," Type 3.210.....	795.00

FIXED DIODE FUNCTION GENERATORS

Dual Log DFG Network, Type 4.120.....	325.00
Dual Log DFG Network "Guaranteed Typical," Type 4.130.....	425.00
Sine Cosine DFG Network, Type 4.510.....	335.00
Sine Cosine DFG Network, "Guaranteed Typical".....	435.00

VARIABLE DIODE FUNCTION GENERATORS

Fixed Breakpoint Variable DFG Network, Type 5.500.....	280.00
Arbitrary DFG Network, Type 5.740.....	370.00

LOGIC INTERFACE

Logic Interface Group, Type 9.000 w/ 1 ea Dual Comparators, Type 9.110 1 ea 3 pole double throw relay and driver, Type 9.410 1 ea Dual Electronic Switching Network, Type 9.230 1 ea Dual Track and Store Unit, Type 9.310.....	515.00
Comparator, Type 9.100.....	135.00
3 pole relay and driver, Type 9.410.....	55.00
Dual Electronic Switching Network, Type 9.230.....	170.00
Dual Track and Store Units, Type 9.310.....	65.00

FUNCTION SWITCHES

Push Button Function Switch, Type 9.750.....	35.00
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LIMITERS AND DIODES

Hard Limiter, Type 6.140.....	39.00
Zero Limiter, Type 6.200.....	20.00
Free Diodes, Type 6.000.....	5.00

Prices are subject to change without notice and are F.O.B. Northbrook, Illinois